

This diagram shows a cross-sectional view of a substrate assembly. It consists of a base substrate 4 with a top layer 11. Two solder bumps 13 are mounted on the top layer 11, each sitting on a pad 10. The bumps 13 are connected to a conductive layer 16. A side layer 12 is on the right side, and a gap 6 is shown between the side layer and the base substrate. A reference numeral 29 points to the base substrate 4.

FIG.2

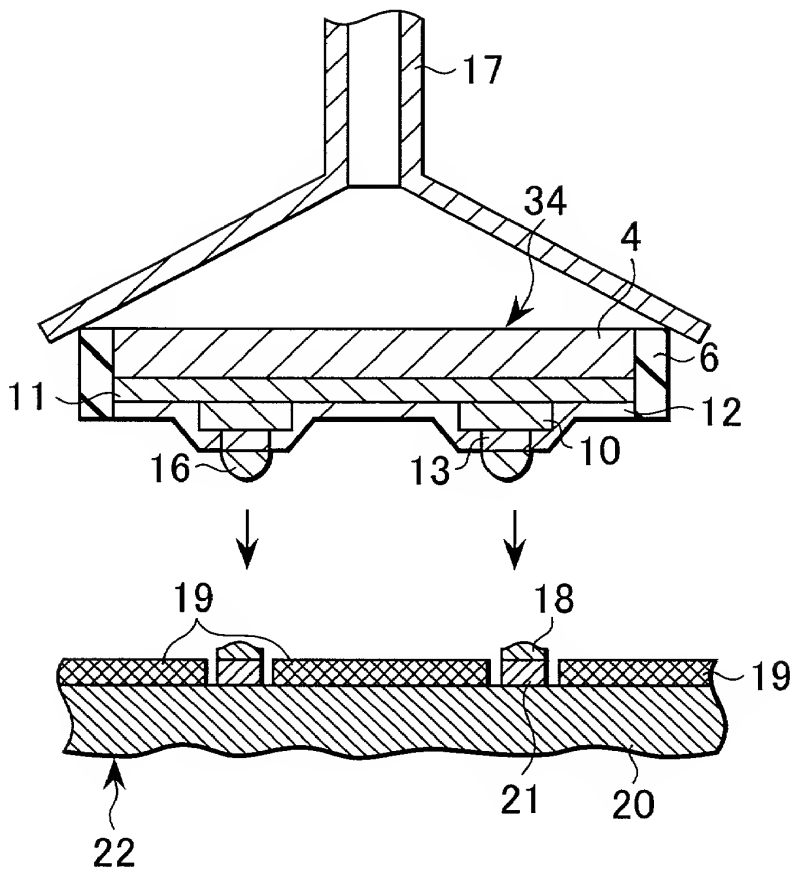


FIG.3

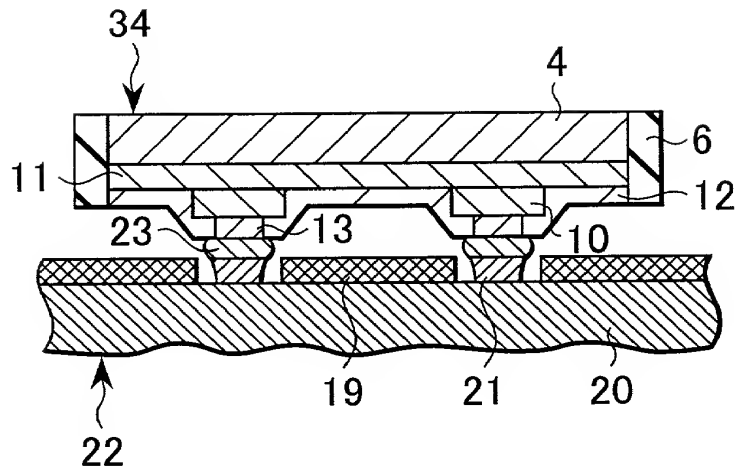


FIG.4

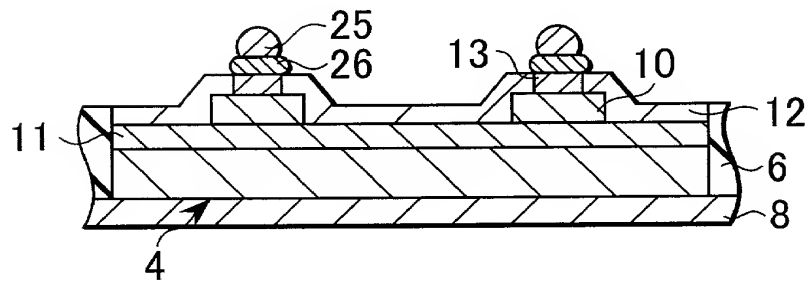


FIG.5

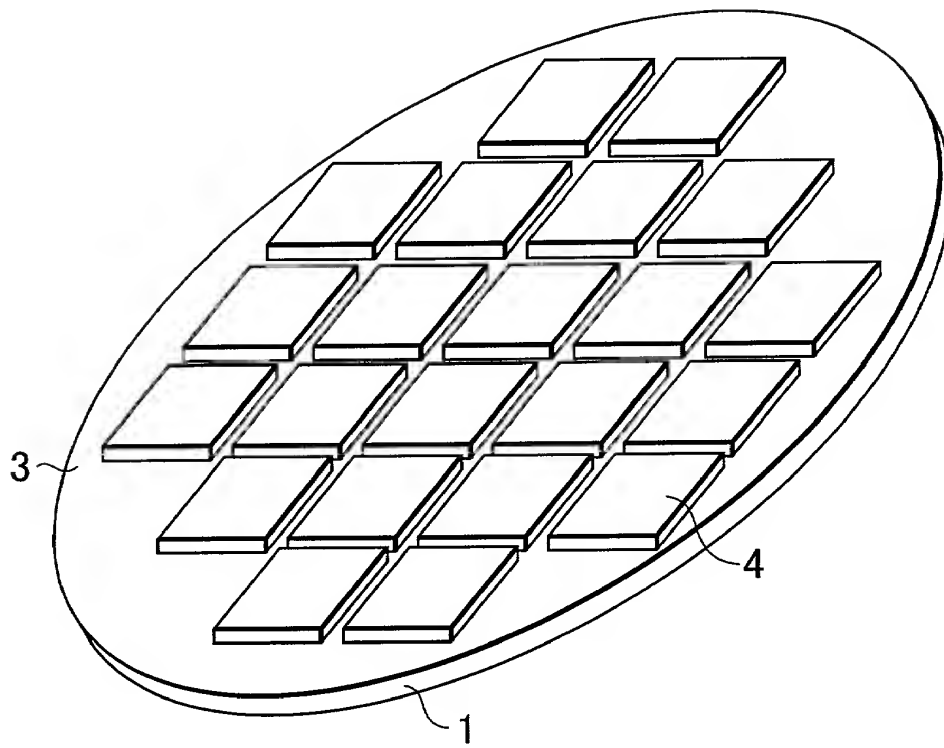


FIG.6

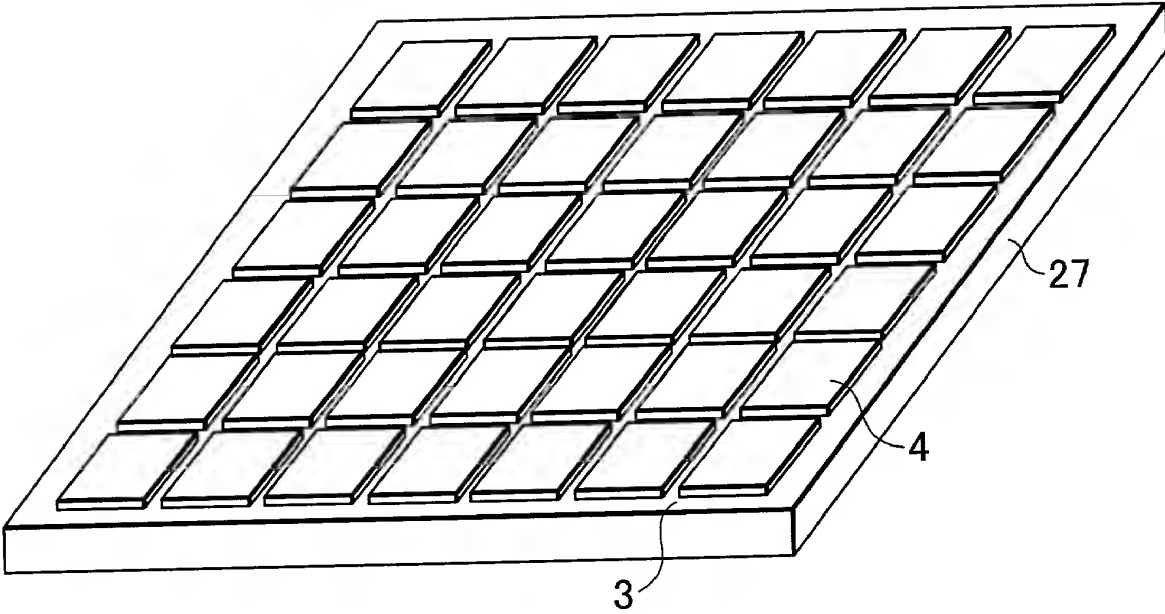


FIG.7

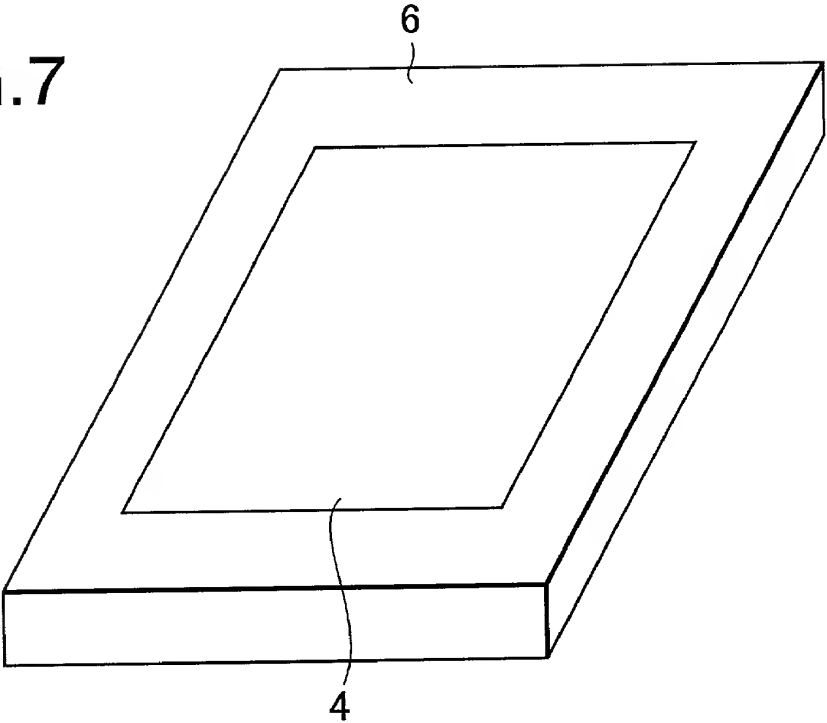


FIG.8

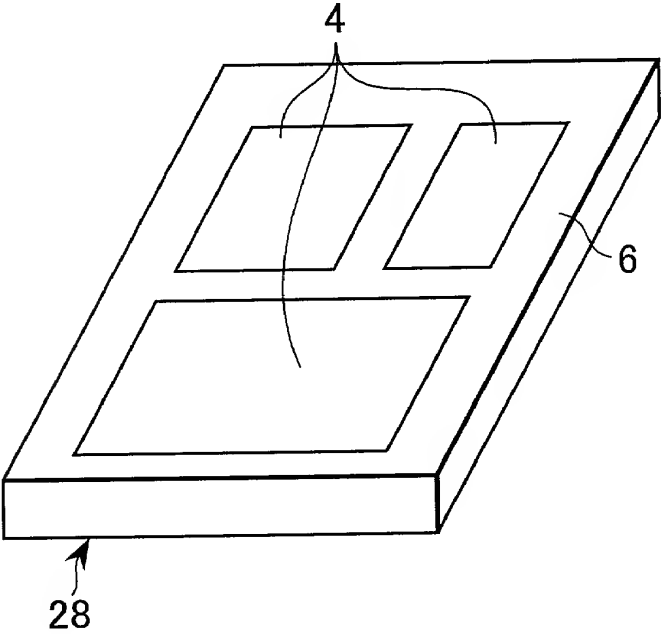
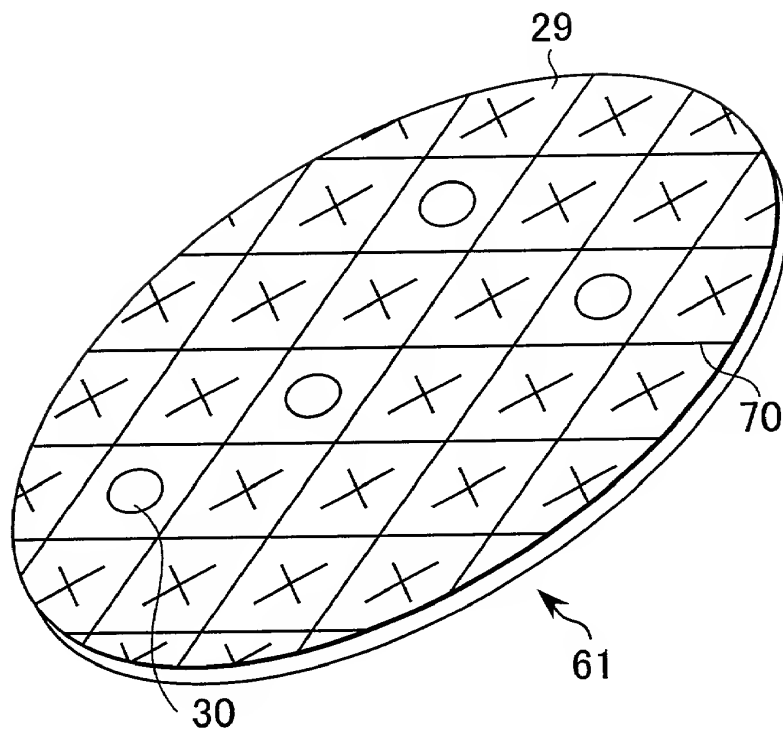




FIG.9



○:NON-DEFECTIVE CHIP

×:DEFECTIVE CHIP

FIG.10A

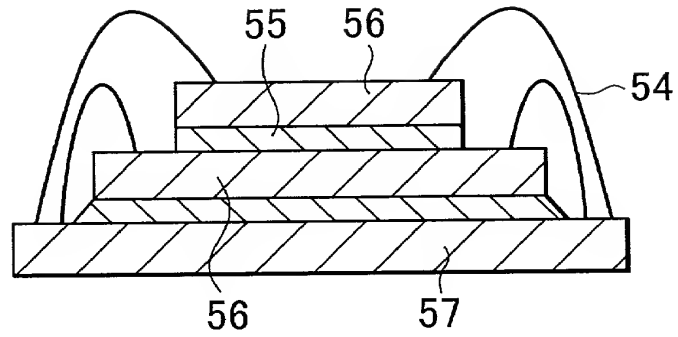


FIG.10B

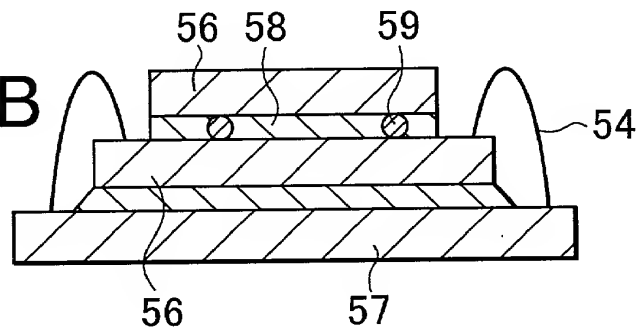


FIG.10C

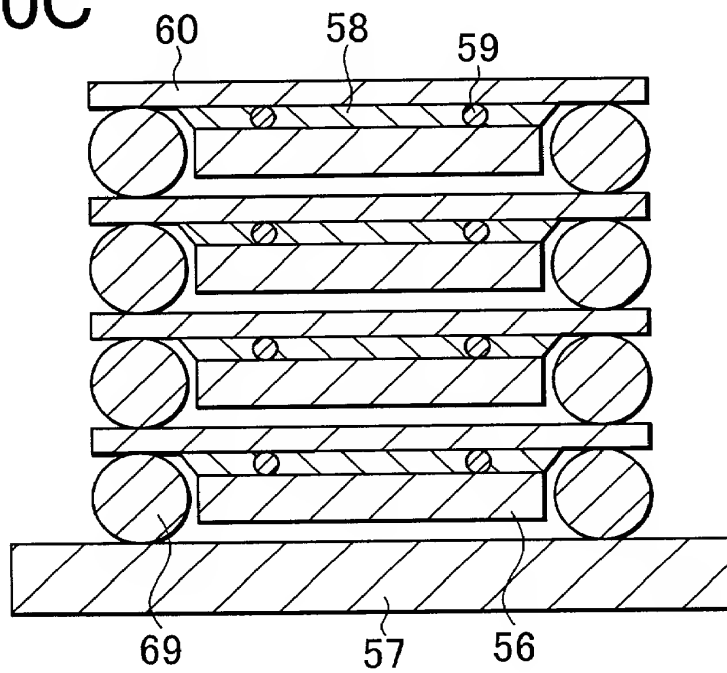


FIG.11A

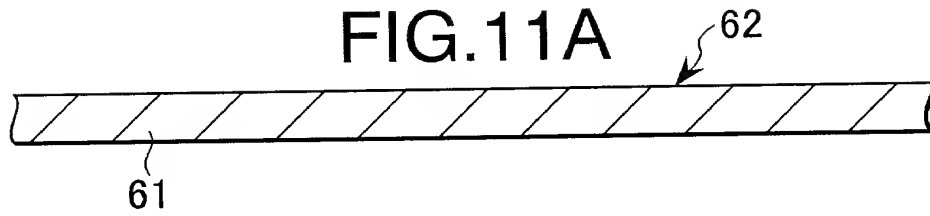


FIG.11B

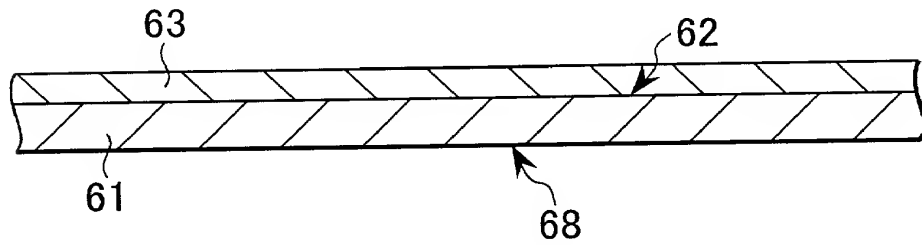


FIG.11C

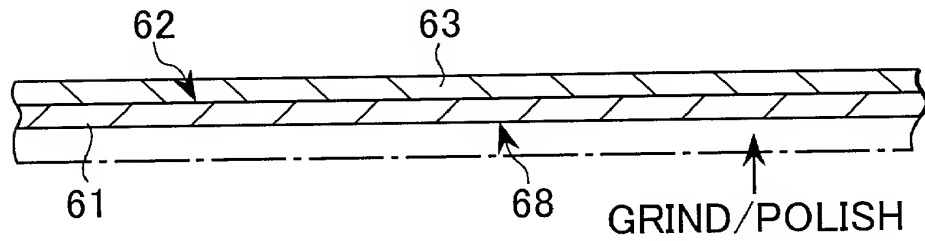


FIG.11D

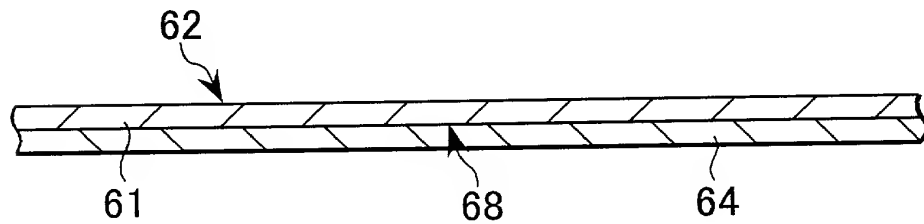


FIG.11E

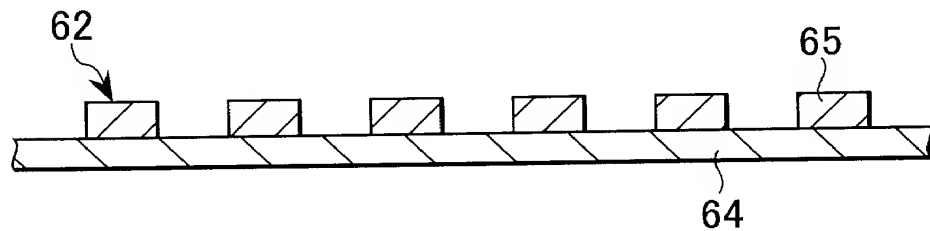


FIG.12A

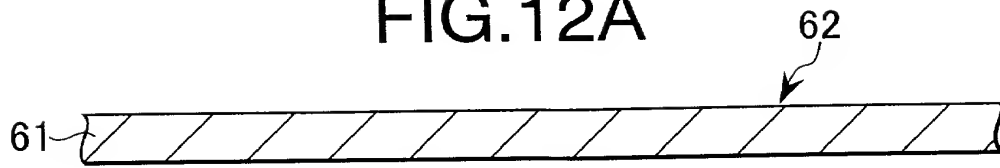


FIG.12B

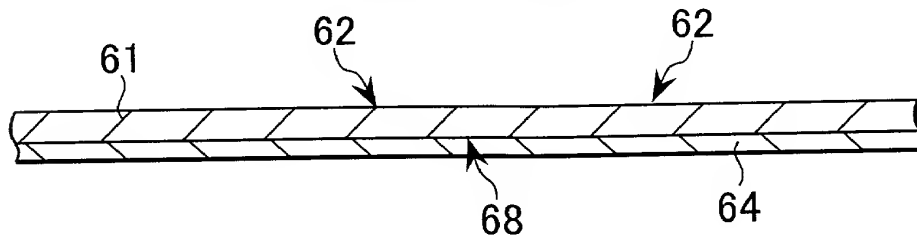


FIG.12C

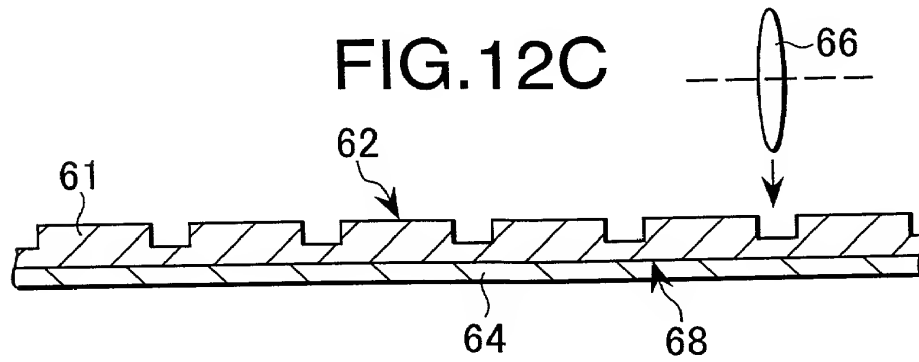


FIG.12D

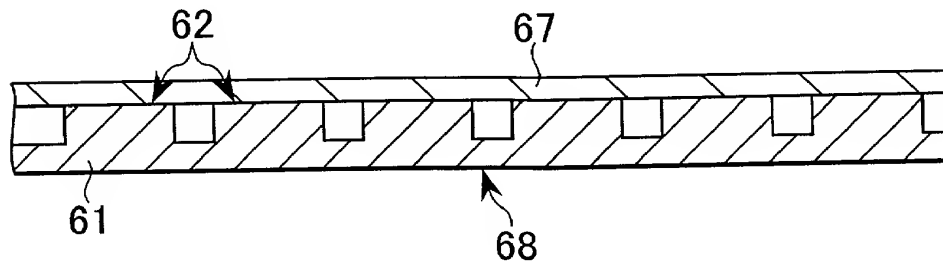


FIG.12E

